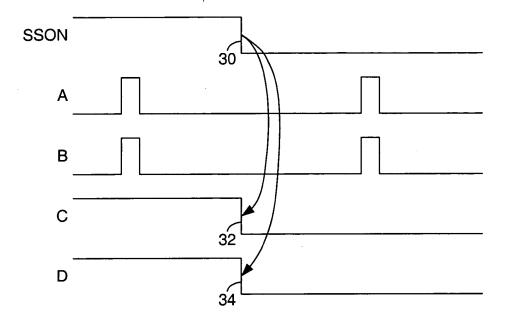


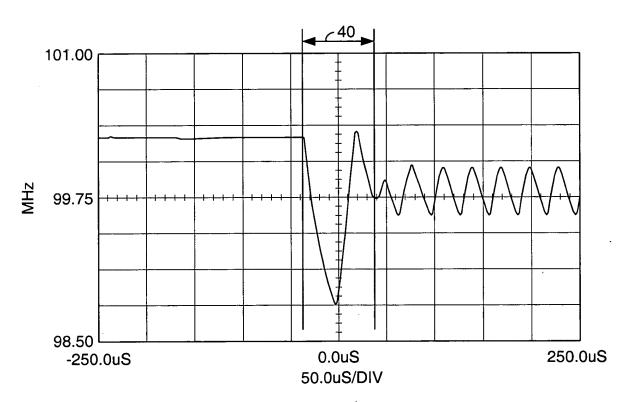
FIG. 1

100 -114 REF 0 -112 SSON_A -110 ¹118 122 \$\$0N° 104√ 115ղ **FDBCK** CPU/ **SYNCHRONIZER MODULATOR MOTHERBOARD** ¹116 126 ¹\106 SSON_B 120 124-125

FIG. 3







(CONVENTIONAL) FIG. 2



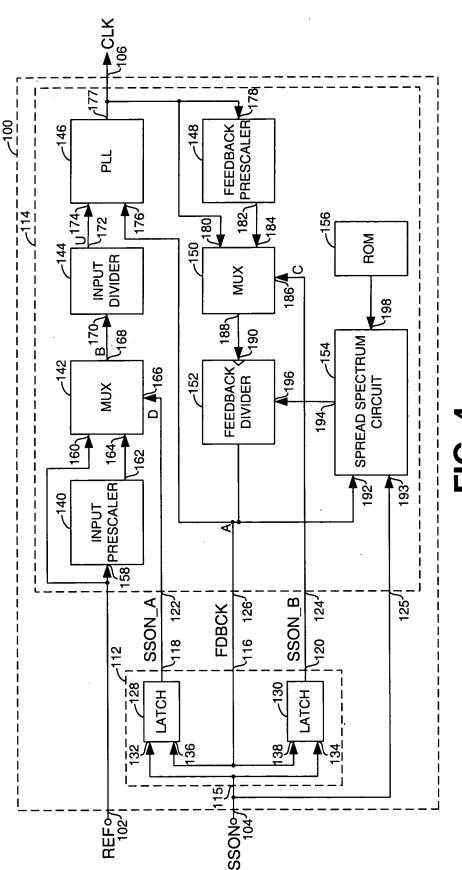


FIG. 4



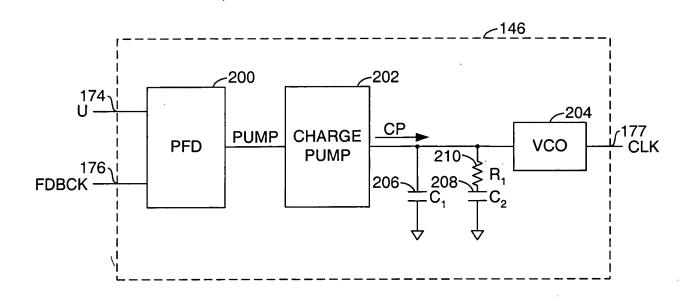
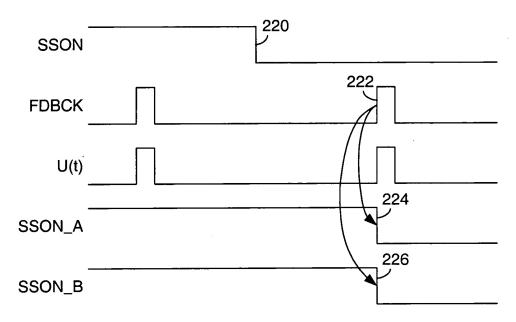


FIG. 5





SPREAD SPECTRUM TRANSITION BEHAVIORS ARE CONTROLLED BY THE PROGRAM

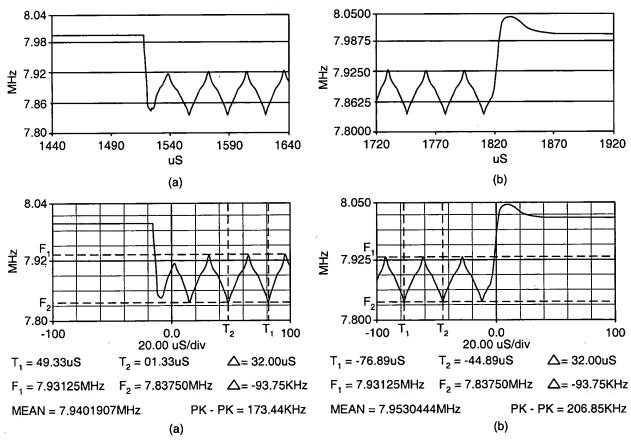
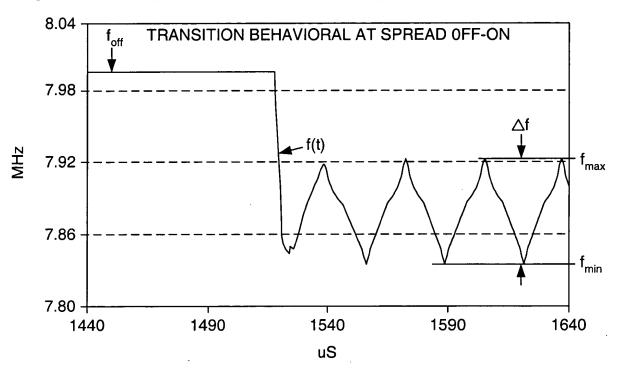


FIG. 6



CRITERIA FOR DETERMINING "GOOD AND BAD" SS TRANSIENT BEHAVIOR



f(t): PLL's RUNNING FREQUENCY IN TRANSIENT PERIOD

for : PLL's SSCG OFF FREQUENCY

 \mathbf{f}_{max} : MAXIMUM FREQUENCY IN SSCG ON

 \mathbf{f}_{\min} : MINIMUM FREQUENCY IN SSCG ON

△f: PEAK TO PEAK FREQUENCY IN SSCG

CRITERIA NEED TO BE SATISFIED:

FREQUENCY RUNNING RANGE DURING TRANSIENT $f_{min} \le f(t) \le f_{off}$

FIG. 7



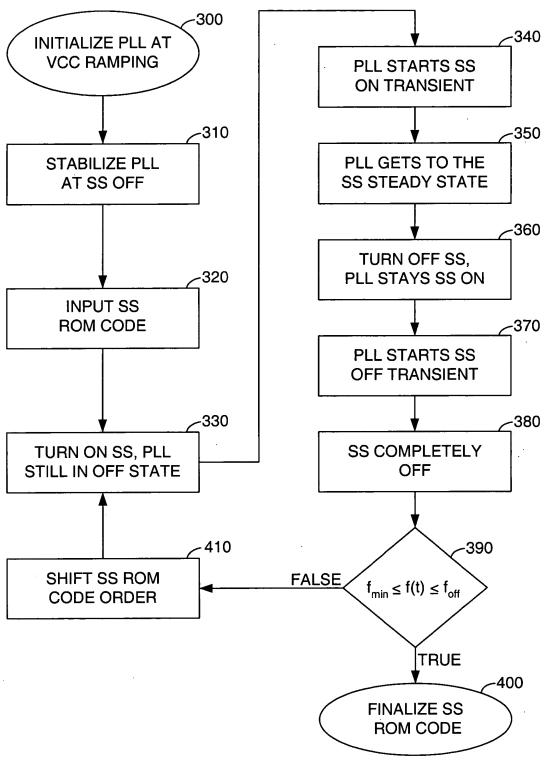
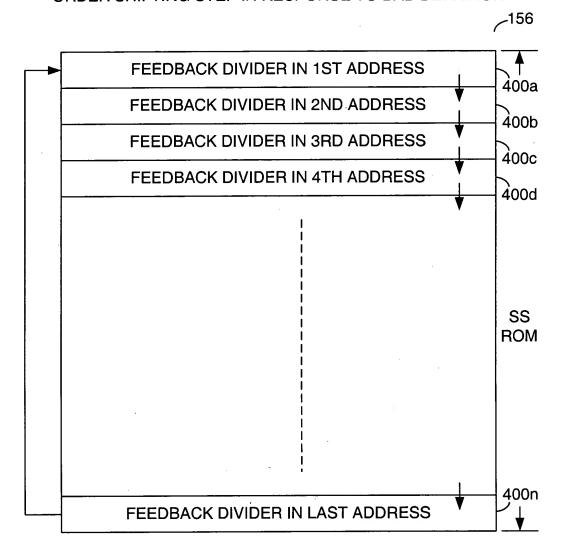


FIG. 8



ORDER SHIFTING STEP IN RESPONSE TO BAD BEHAVIOR



MOVE FEEDBACK DIVIDER IN LAST ADDRESS TO 1ST ADDRESS AND SHIFT DOWN SS ROM CODE.

FIG. 9